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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,171	09/04/2001	Ming-Dou Ker	0941-0316P-SP	9842

2292 7590 02/14/2008

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EXAMINER	
JACKSON JR, JEROME	
ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
02/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	09/944,171	KER ET AL.	
	Examiner	Art Unit	
	Jerome Jackson Jr.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 27-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is no standard “MOS” structure. The exact structure of the claim is vague and indefinite. The recitation “MOS of the first conductivity type” is vague and indefinite because field effect transistors can be enhancement mode, depletion mode, n-channel, p-channel, etc., have n-type source and drain regions with a p-type channel, p-type source and drain regions with a p-type channel, etc. “MOS of a first conductivity type” does not define a particular field effect transistor structure with enough specificity for one of ordinary skill to understand the exact metes and bounds of the claimed structure. What comprises the “first conductivity type”, the source and drain, the channel, both, or what ? The claim is vague and indefinite. Other claims are vague and indefinite for dependence on the rejected base claim. Furthermore, abreviations such as "MOS" do not particularly define a structure. Acronyms may define different structures. There is no specific structure claimed particularly defining "MOS". At best “MOS” alone, here, is considered a mere vague and indefinite label.

Claims 2,3,27,34 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Efland, of record.

The previous rejection still applies. The protection circuit of Efland is clearly formed between power lines Vs and ground and the I/O pad attached the gates of the device or else the protection circuit would not work. Applicant is invited to comment on how else the protection device of Efland could possibly be connected if not precisely in this manner. See figure 16 where the applied gate voltage Vg is located precisely between the power lines and the protection circuit comprising the protection diodes. There has to be an input pad to apply Vg. Does applicant know of any other method to apply a voltage to an integrated circuit ? Clearly applicant must at least consider an I/O pad to be an obvious structure to apply voltages such as Vg to the integrated circuitry. Applicant's own prior art admissions in figures 1a and 1b, for example, show pads 10, Vss and Vdd. These are fundamental in the art.

Efland, as stated previously, also shows in figures 16 and 17, doped area 213 of first conductivity type (N) in a first well 209 of second conductivity type (P), and a deep well of N conductivity type under the first well to isolate the first well from the substrate. There are a plurality of protection diodes and they function in the same manner claimed or else they would not be able to protect the device. Note also the number of protection diodes is dependent on the required voltage protection with diodes having a forward voltage of approximately 0.7 V and a reverse Zener voltage of 8-9 V. The protection diodes are strung together to provide the necessary protection. A plurality of diodes for protection from spikes on either power line is disclosed and fundamental in the protection art. Claims 2 and 3 are rejected.

Claim 27 is rejected because the plurality of protection diodes in Efland are also located between the first power line, Vs, and the second power line, ground, and comprise a "further" "power-rail ESD clamp circuit". The plurality of protection diodes function in the manner claimed.

Claim 34 is rejected as the protection diode regions of Efland can be likewise labeled as "source/drain" or "substrate" region of a "MOS". They are mere labels here for diode regions.

Claims 2, 3 and 27-34, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Efland in view of Horiguchi, 5,932914, and applicant's prior art admissions (APA).

Efland discloses protection diodes in isolated wells without any field effect transistor gate structure. Horiguchi discloses protection diodes or parasitic bipolar elements formed from field effect transistor structure in isolated wells. The wells are similar to wells in Efland. The parasitic bipolar diode based structure is excellent for protecting devices. See column 2 and the figures of Horiguchi. It would have been prima facie obvious to have practiced protection strings of diodes as Efland formed from field effect transistor elements as shown in Horiguchi because the parasitic protection bipolar diode structure affords excellent protection. Claim structure reciting any "MOS" structure is shown by Horiguchi and is therefore obvious. The functional language also does not distinguish over the prior art functioning in the same manner. In regard to structure or any argument concerning "further" clamp circuits or protection devices between both power lines, applicant's own admissions show protection devices so located, and clearly

providing protection devices as Efland, or Efland with Horiguchi, between both power lines and input pads would have been prima facie obvious. See APA prior art figures. See also Efland showing diodes between power line Vs and power line “ground”.

Applicant's arguments filed 11/29/07 have been fully considered but they are not persuasive. Arguments regarding the board decision are not convincing because new art was used in the rejection.

Arguments regarding Efland are not convincing because Vg is applied to an I/O pad. Voltages are applied through I/O pads in integrated circuits. Does applicant know any other way to apply voltages to integrated circuits, and in any event, APA shows I/O pads. I/O pads to apply voltages are clearly obvious structure and clearly would have been obvious structure to apply voltage Vg in Efland. The second power line in Efland is ground and the first is Vs as stated above. To apply the ground or Vs “power” voltages it would have been clearly obvious or necessary to use “lines” and "pads".

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 571-272-1730. The examiner can normally be reached on M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815